FAULT-TOLERANT MULTI-CORE MICROPROCESSING

ABSTRACT OF THE DISCLOSURE

One embodiment disclosed relates to a method of executing program code on a target microprocessor with multiple CPU cores thereon. One of the CPU cores is selected for testing, and inter-core context switching is performed. Parallel execution occurs of diagnostic code on the selected CPU core and the program code on remaining CPU cores. Another embodiment disclosed relates to a microprocessor having a plurality of CPU cores integrated on the microprocessor chip. Inter-core communications circuitry is coupled to each of the CPU cores and configured to perform context switching between the CPU cores.